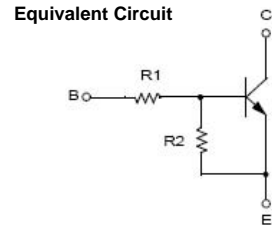
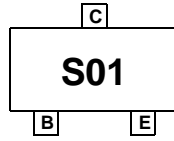
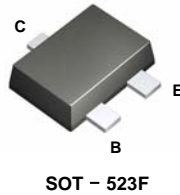


FJY3001R

NPN Epitaxial Silicon Transistor

Features

- Switching circuit, Inverter, Interface circuit, Driver Circuit
- Built in bias Resistor (R1=4.7KΩ, R2=4.7KΩ)
- Complement to FJY4001R



Absolute Maximum Ratings* $T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	50	V
V_{CEO}	Collector-Emitter Voltage	50	V
V_{EBO}	Emitter-Base Voltage	10	V
I_C	Collector Current	100	mA
T_{STG}	Storage Temperature Range	-55~150	$^\circ\text{C}$
T_J	Junction Temperature	150	$^\circ\text{C}$
P_C	Collector Power Dissipation, by $R_{\theta JA}$	200	mW

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics* $T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	600	$^\circ\text{C/W}$

* Minimum land pad size.

Electrical Characteristics* $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	MIN	Typ	MAX	Units
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 10 \mu\text{A}, I_E = 0$	50			V
$V_{(BR)CEO}$	Collector-Base Breakdown Voltage	$I_C = 100 \mu\text{A}, I_B = 0$	50			V
I_{CBO}	Collector-Cutoff Current	$V_{CB} = 40 \text{V}, I_E = 0$			0.1	μA
h_{FE}	DC Current Gain	$V_{CE} = 5 \text{V}, I_C = 10 \text{mA}$	22			
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 10 \text{mA}, I_B = 0.5 \text{mA}$			0.3	V
f_r	Current Gain - Bandwidth Product	$V_{CE} = 10 \text{V}, I_C = 5 \text{mA}$		250		MHz
C_{cb}	Output Capacitance	$V_{CB} = 10 \text{V}, I_E = 0, f = 1.0 \text{MHz}$		3.7		pF
$V_{I(off)}$	Input Off Voltage	$V_{CE} = 5 \text{V}, I_C = 100 \mu\text{A}$	0.5			V
$V_{I(on)}$	Input On Voltage	$V_{CE} = 0.3 \text{V}, I_C = 20 \text{mA}$			3	V
R_1	Input Resistor		3.2	4.7	6.2	KΩ
R_1/R_2	Resistor Ratio		0.9	1.0	1.1	

* Pulse Test: $PW \leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$

Typical Performance Characteristics

Figure 1. DC current Gain

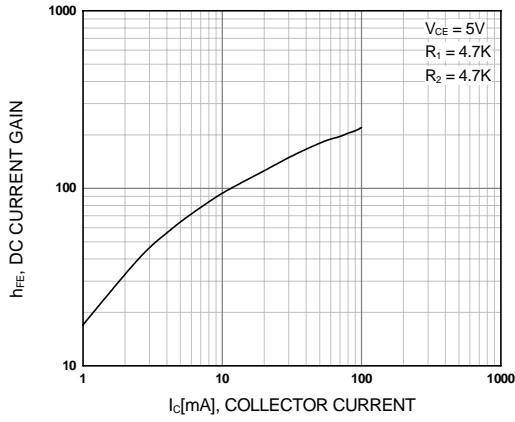


Figure 2. Input On Voltage

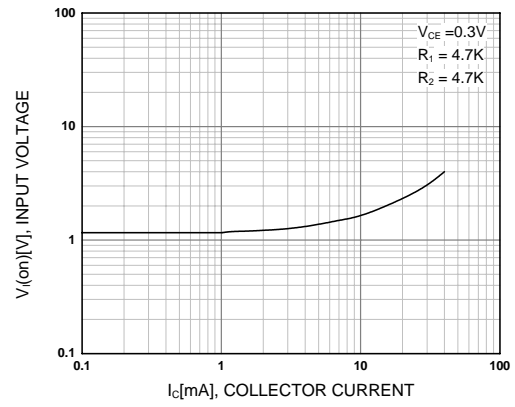


Figure 3. Input off Voltage

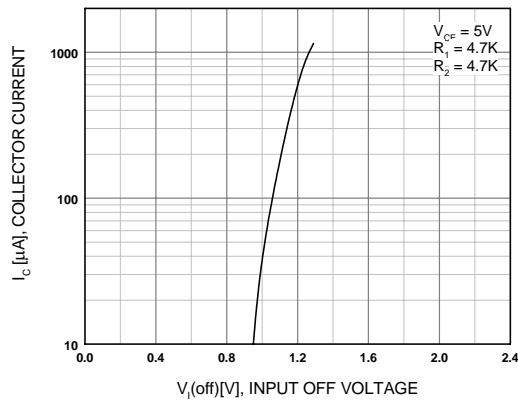
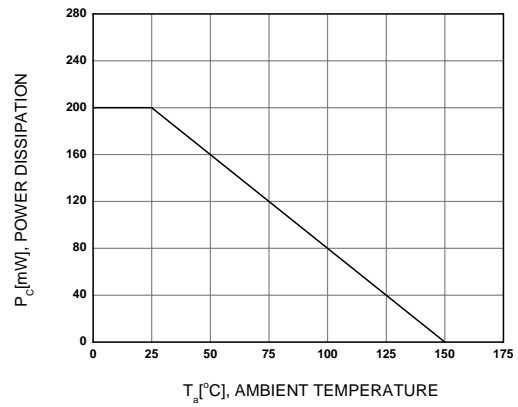
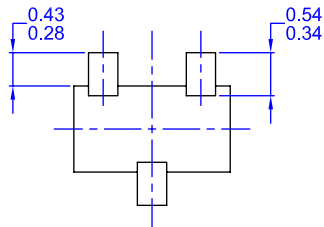
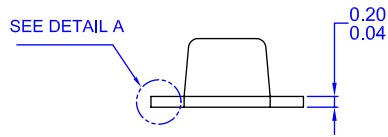
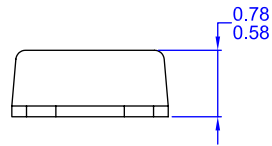
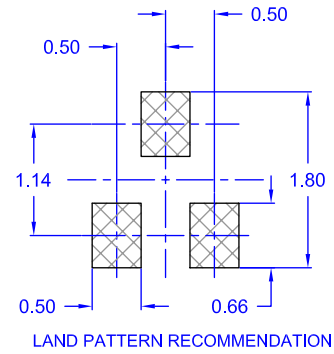
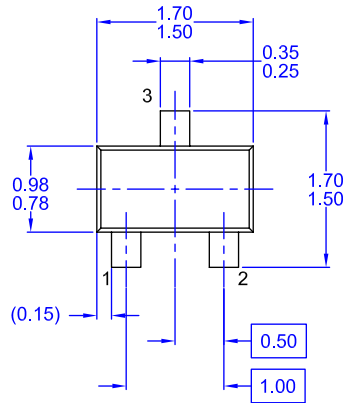


Figure 4. Power Derating



Package Dimensions

SOT-523F




NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO EIAJ SC89 PACKAGING STANDARD.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

Dimensions in Millimeters



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FACT®	OPTOPLANAR®	SuperSOT™-3	
FAST®	PACMAN™	SuperSOT™-6	
FASTr™	PDP-SPM™	SuperSOT™-8	
FPS™	POP™	SyncFET™	
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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